RICKI TURA

Electronic Engineer

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PROFILE

Hardware Verification Engineer and former UKESF Scholar of the Year with experience in UVM, flow development, and automation with Jenkins.

EXPERIENCE

Hardware Verification Engineer

Tessent Embedded Analytics (formerly UltraSoC) - Siemens

June 2020 – Present Bristol, UK

- Verification of three IP blocks with UVM testbenches.
- Mentored student interns on verification projects involving coverage agents, coverage collection, and assertions.
- Creating common UVM component libraries for self registering interfaces with sequence-based API.
- Developed YAML -> Jenkins -> Questa-VRM -> Questa-VIQ flow for nightly testing of IP blocks.
- Use of Ansible (Infrastructure as Code) to maintain desktop and grid machines, license servers, Jenkins, and VIQ.
- Regular collaboration with Questa-VIQ team to test new features and suggest improvements.
- Various improvements to GNU Make flow for running local regressions and other tools such as synthesis (Genus) and unreachability (JasperGold).
- Managed IP Release Flow in Jenkins, various refactors and rework in Python and Groovy.
- Creator of the Early Career Engineers group within the Hardware team. Used to discuss recent papers/presentations, professional development, and trial ideas before presenting to the wider team.
- Maintainer of the Hardware team's Confluence (Wiki). Regular publisher of how-to guides on new methodologies, flows, and processes.

UKESF Industrial Placement Student

UltraSoC Technologies

June 2018 – June 2019 Cambridge, UK

A year long placement as part of the Industrial Studies section of my MEng and participation of the UKESF scheme.

- Python, Perl, and TCL scripting for regression testing.
- XML transformations to generate Word documents.
- Creating a UVM environment and writing verification tests.
- Python, Django, MySQL, and Jenkins to create a GUI.
- Creating SystemVerilog modules to provide UVM generated stimulus in a Python-built sub-system environment.
- Creating an automatic FPGA build and regression testing system using Jenkins, Python, and Xilinx Vivado.
- Weekly lessons in Mandarin Chinese.

STRENGTHS

SystemVerilog | UVM | Jenkins-Groovy | Questa-VRM | Questa-VIQ | Polarion | Ansible | Git/Gitlab | Python

EDUCATION

MEng Electrical and Electronic Engineering with Industrial Studies

National University of Singapore

January 2020 – May 2020

University of Southampton

Sept 2015 – December 2019

First class integrated Masters degree with a 12 month work placement and a semester exchange.

MEng Thesis: 4G/5G Demonstrator for NI USRP (software defined radio)

BEng Thesis: Design and implementation of autonomous coupling and additional features for the SwarmIR platform

A-Levels and GCSEs

Thomas Deacon Academy, Peterborough

A* – Mathematics, Physics, Chemistry
A (AS) – Further Maths, Economics, EPQ
ELC Grade 3 - Mandarin Chinese

Thomas Clarkson Academy, Wisbech

A* – 9 including English and Maths

PROGRAMS

UKESF Scholar

UK Electronics Skills Foundation

January 2016 - May 2020

- Work placements at Micron (2016) and UltraSoC Technologies (2017 & 2018).
- Supported younger UKESF Scholars through a buddy scheme, offering guidance and advice.
- Promoted electronics in schools and sixth forms.

President

Electronics and Computer Science Society

April 2016 - April 2018

Directed the University student society and developed relationships with the faculty, sponsors, and 2000+ members.