RICKI TURA

Electronic Engineer

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PROFILE

Hardware Verification Engineer experienced in UVM, RISC-V, and block/core verification with a strong passion for building robust automated flows.

EXPERIENCE

Verification Engineer

Codasip

October 2023 – Present Bristol, UK

- Core-level verification of an in-order CPU using STING, randomised memory maps, assertions, and directed testing.
- Block-level verification of an out-of-order CPU. UVM environment with models and agents to verify the Instruction Renamer and Reorder Buffer.
- Bespoke RISC-V architectural coverage collection tool with generated covergroups and sampling based on YAML input parameters. Used in multiple projects and scalable.
- Packaging flow for deliverable RTL, SDK, documentation, and CI out-of-box testing with multiple simulators and benchmarks. Hands-on experience with synthesis tools, netlist simulations, ELF compilers, and linker scripts.
- Dead code analysis with Questa CoverCheck. Interfaced with GNU Make flow and deployed in nightly testing on multiple benches to close coverage.
- Mentored UKESF scholars during summer internships and scoped engaging tasks for them to complete.

Hardware Verification Engineer

Tessent Embedded Analytics (formerly UltraSoC) - Siemens

June 2020 – October 2023 Bristol, UK

- Verification of three IP blocks with UVM testbenches.
- Creating common UVM component libraries for self registering interfaces with sequence-based API.
- Developed YAML -> Jenkins -> Questa-VRM -> Questa-VIQ flow for nightly testing of IP blocks.
- Use of Ansible (Infrastructure as Code) to maintain desktop and grid machines, license servers, Jenkins, and VIQ.
- Managed IP Release Flow in Jenkins, various refactors and rework in Python and Groovy.
- Mentored student interns on verification projects involving coverage agents, coverage collection, and assertions.

UKESF Industrial Placement Student

UltraSoC Technologies

June 2018 – June 2019 Cambridge, UK

A year long placement as part of the Industrial Studies section of my MEng and UKESF scholarship scheme.

STRENGTHS

SystemVerilog · UVM · RISC-V · Python · Questa · VCS · CoverCheck · Polarion · GitLab CI · Ansible · Slurm · AsciiDoc

EDUCATION

MEng Electrical and Electronic Engineering with Industrial Studies

University of Southampton

Sept 2015 – May 2020

First class integrated Masters degree with a 12 month work placement and a semester exchange at the National University of Singapore.

MEng Thesis: 4G/5G Demonstrator for NI USRP (software defined radio)

BEng Thesis: Design and implementation of autonomous coupling and additional features for the SwarmIR platform.

President of the Electronics and Computer Science Society. Directed events and strategy with the faculty and sponsors for our 2000+ members.

A-Levels

Thomas Deacon Academy, Peterborough

A* – Mathematics, Physics, Chemistry
A (AS) – Further Maths, Economics, EPQ
ELC Grade 3 - Mandarin Chinese

INTERESTS

UKESF Board Observer

UK Electronics Skills Foundation

June 2022 - Present

Long-standing involvement with the UK's leading charity for electronics skills, from scholarship recipient to board observer:

- Internships at Micron (2016) and UltraSoC Technologies (2017 & 2018).
- Named the 2018 UKESF Scholar of the Year at the TechWorks awards.
- Promoted electronics in schools and sixth forms.
- Supporting current UKESF Scholars through a buddy scheme, offering guidance and advice.

Half Marathons · Houseplants · Drum & Bass